What is claimed is:

1. An integrated circuit comprising:

an interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals; and

during the second mode of operation, the first transceiver is capable of only transmitting signals and the second transceiver is capable of only receiving signals.

2. The integrated circuit of claim 1 wherein a control logic, coupled to the integrated circuit, is capable of generating a control signal and wherein the integrated circuit operates in the first mode of operation responsive to the control signal.

3. The integrated circuit of claim 2 wherein the control signal is generated in response to a number of times the first transceiver transitions between transmitting and receiving during a period of time.

4. The integrated circuit of claim 2 wherein the control signal is generated in response to a number of transmit commands and a number of receive commands.

5. The integrated circuit of claim 2 wherein the control signal is generated in response to a user selectable setting at initialization.

6. The integrated circuit of claim 2 wherein the control signal is generated in response to a user selectable setting during normal operating mode.

7. The integrated circuit of claim 4 wherein the control signal is generated in response to a priority of the data.

8. The integrated circuit of claim 2 wherein the control signal is generated in response to a number of transmit data packets and a number of receive data packets.

9. The integrated circuit of claim 8 wherein the control signal is generated in response to a priority of the data.

10. The integrated circuit of claim 2 wherein the control logic is included in another integrated circuit and the control logic has information regarding bandwidth requirements.

11. The integrated circuit of claim 2 wherein the control logic includes executable instructions.

12. The integrated circuit of claim 11 wherein the executable instructions are included in an application software program.

13. The integrated circuit of claim 11 wherein the executable instructions are included in an operating software program.

14. The integrated circuit of claim 11 wherein the executable instructions are included in firmware.

15. The integrated circuit of claim 2 wherein the control signal is generated in response to a number of data packets waiting to be transmitted.

16. The integrated circuit of claim 2 wherein the control signal is generated in response to a number of data packets waiting to be received.

17. The integrated circuit of claim 2 wherein the control signal is generated in response to an average time a data packet waits to be transmitted.

18. The integrated circuit of claim 2 wherein the control signal is generated in response to a power consumption of the integrated circuit.

19. The integrated circuit of claim 2 wherein the control signal is generated in response to a temperature of the integrated circuit.

20. The integrated circuit of claim 2 wherein the control signal is generated in response to a first statistic obtained during a first period of time and a second statistic obtained during a second period of time.

21. The integrated circuit of claim 2 wherein the integrated circuit is capable of generating a first bandwidth request and another integrated circuit is capable of generating a second bandwidth request, and wherein the control signal is generated in response to the first bandwidth request and the second bandwidth request.

22. The integrated circuit of claim 2 wherein the integrated circuit is capable of generating a first temperature signal representing the temperature of the integrated circuit and another integrated circuit is capable of generating a second temperature signal representing the temperature of another integrated circuit, and wherein the control signal is generated in response to the first temperature signal and the second temperature signal.

23. The integrated circuit of claim 2 wherein the control signal is generated periodically.

24. The integrated circuit of claim 2 wherein the control logic generates a control signal in response to an override signal.

25. The integrated circuit of claim 2 wherein the control logic generates a control signal in response to a threshold value.

26. The integrated circuit of claim 25 wherein the threshold value is a minimum bandwidth.

27. The integrated circuit of claim 25 wherein the threshold value is a maximum temperature value.

28. The integrated circuit of claim 25 wherein the threshold value is a maximum power consumption value.

29. The integrated circuit of claim 25 wherein the threshold value is a number of times the first transceiver transitions between transmitting and receiving during a period of time.

30. The integrated circuit of claim 25 wherein the threshold value is a minimum latency value.

31. The integrated circuit of claim 2 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is disabled for transmitting or receiving signals.

32. The integrated circuit of claim 31 wherein the third mode of operation is a phase calibration mode.

33. The integrated circuit of claim 31 wherein the third mode of operation is an impedance calibration mode.

34. The integrated circuit of claim 31 wherein the second transceiver is disabled responsive to power constraint.

35. The integrated circuit of claim 31 wherein the second transceiver is disabled in response to a hardware device failure.

36. The integrated circuit of claim 31 wherein the second transceiver is disabled in response to a signal failure.

37. The integrated circuit of claim 2 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver is capable of only transmitting signals and the second transceiver is disabled.

38. The integrated circuit of claim 2 wherein the integrated circuit is operable in a third mode,

wherein:

during the third mode of operation, the first transceiver is capable of only receiving signals and the second transceiver is disabled.

39. The integrated circuit of claim 38 wherein the third mode of operation is a phase calibration mode.

40. The integrated circuit of claim 38 wherein the third mode of operation is an impedance calibration mode.

41. The integrated circuit of claim 2 wherein the control signal is selected from the group consisting of an address/data strobe, write enable signal, chip select signal, data valid signal, or data ready signal.

42. The integrated circuit of claim 2 wherein the first transceiver and second transceiver are coupled to an input multiplex deserializer circuit and an output multiplex serializer circuit.

43. A circuit comprising:

an interface having a plurality of contacts including a first set of contacts and a second set of contacts; and,

control logic, coupled to the interface, capable of configuring the first set of contacts to transmit and the second set of contacts to receive.

44. The circuit of claim 43 wherein the plurality of contacts include a third set of contacts and wherein the control logic is capable of configuring the third set of contacts to transmit and receive.

45. The circuit of claim 43 wherein the plurality of contacts include a third set of contacts and wherein the control logic is capable of configuring the third set of contacts to be disabled.

46. A circuit comprising:

an interface having a plurality of contacts including a first set of contacts, a second set of contacts, a third set of contacts and a fourth set of contacts; and,

control logic, coupled to the interface, capable of configuring the first set of contacts to transmit, the second set of contacts to receive, the third set of contacts to transmit and receive and the fourth set of contacts to be disabled.

47. A memory system comprising:

an input/output connector interface capable of adaptively or user-defined partitioning a plurality of contacts into unidirectional contacts and bidirectional contacts responsive to a control signal; and,

control logic, coupled to the input/output connector interface, capable of outputting the control signal.

48. The memory system of claim 47 wherein the unidirectional contacts include a first contact for only receiving a first signal and a second contact for only transmitting a second signal.

49. The memory system of claim 47 wherein the plurality of contacts include maintenance contacts that are disabled responsive to the control signal.

50. An apparatus comprising:

a first integrated circuit including,

a first contact coupled to a first transceiver;

a second contact coupled to a second transceiver;

wherein the first integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals;

during the second mode of operation, the first transceiver is capable of transmitting signals and the second transceiver is capable of receiving signals; and,

a second integrated circuit, coupled to the first integrated circuit, including,

a first contact coupled to a first transceiver;

a second contact coupled to a second transceiver;

wherein the second integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals;

during the second mode of operation, the first transceiver is capable of receiving signals and the second transceiver is capable of transmitting signals.

51. The apparatus of claim 50 further comprising:

a third integrated circuit, coupled to the first integrated circuit and the second integrated circuit, including,

a first contact coupled to a first transceiver;

a second contact coupled to a second transceiver;

wherein the third integrated circuit is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals;

during the second mode of operation, the first transceiver is capable of receiving signals and the second transceiver is capable of transmitting signals.

52. The apparatus of claim 50 wherein the apparatus is a general-purpose computer.

53. The apparatus of claim 50 wherein the apparatus is a coprocessor.

54. The apparatus of claim 50 wherein the apparatus is a video game console.

55. The apparatus of claim 50 wherein the apparatus is a computer graphics card.

56. The apparatus of claim 50 wherein the apparatus is a printer.

57. An apparatus comprising:

a master device including,

a connector interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the master device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals;

during the second mode of operation, the first transceiver is capable of only transmitting signals and the second transceiver is capable of only receiving signals; and,

a memory, coupled to the master device, including,

a connector interface including a first contact and a second contact;

a first transceiver coupled to the first contact;

a second transceiver coupled to the second contact;

wherein the memory is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first transceiver is capable of transmitting and receiving signals and the second transceiver is capable of transmitting and receiving signals;

during the second mode of operation, the first transceiver is capable of only receiving signals and the second transceiver is capable of only transmitting signals.

58. The apparatus of claim 57 wherein the master device is a memory controller.

59. The apparatus of claim 57 wherein the master device is a processor.

60. The apparatus of claim 57 wherein the memory is an integrated circuit memory device.

61. The apparatus of claim 57 wherein the memory is a memory module including a plurality of integrated circuit memory devices.

62. The apparatus of claim 57, wherein the master device and memory operate in a first mode of operation responsive to a memory command.